UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/553,529	08/22/2006	Sheila F. Chopin	SC12209TK	1370

23125 7590 03/08/2007

FREESCALE SEMICONDUCTOR, INC.
LAW DEPARTMENT
7700 WEST PARMER LANE MD:TX32/PL02
AUSTIN, TX 78729

EXAMINER	
BARNES, SETH W	
ART UNIT	**PAPER NUMBER**
2822	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/553,529	CHOPIN ET AL.	
	Examiner	Art Unit	
	Seth Barnes	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 October 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 15-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 15-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/14/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Conclusion

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-15 and **19-25** are rejected under **35 U.S.C. 102(b)** as being anticipated by Tsunoda et al. US 5,914,531 (Tsunoda).

Regarding **claim 1**, Tsunoda discloses a method for making a packaged integrated circuit (IC) comprising:

forming a heat spreader (**5**) in a sheet of thermally conductive material (col. **9**, lines **66-67**);

attaching an IC die in a die up configuration to the heat spreader at a first location of the heat spreader (**Fig. 1**);

singulating the heat spreader with the attached IC die from a remaining portion of the sheet wherein the heat spreader extends to at least a portion of an edge of the packaged IC (Fig. **4B (c)**.

Regarding **claim 2**, Tsunoda discloses in **Fig. 1** wherein the forming the heat spreader further includes:

forming a plurality of wire bond windows in the heat spreader located between the first location and an outer portion of the heat spreader (col. **6**, lines **23-31**).

Regarding **claim 3**, Tsunoda discloses in col. **10**, lines **1-3,** wherein forming the wire bond windows further includes forming at least five thermal connection structures thermally coupling the first portion of the heat spreader with the outer portion of the heat spreader, each thermal connection structure defining at least a portion of a wire bond window of the plurality of wire bond windows.

Regarding **claim 4**, Tsunoda discloses in **Fig. 4B (a)** and **(b)**, wherein the forming the heat spreader further includes forming singulation slots in the sheet around an outer portion of the heat spreader, at least portions of the singulation slots being defined by portions of an edge of the outer portion of the heat spreader.

Regarding **claim 5**, Tsunoda discloses in **Fig. 4B** the method of above further comprising:

reducing the thickness of the sheet at a location at an edge of the heat spreader;

wherein the singulating the heat spreader with the attached IC die from a remaining portion of the sheet further includes cutting the sheet at the location at the edge of the outer portion.

Regarding **claim 6**, Tsunoda discloses in col. **6**, line **65** – col. **7**, line **28** the method above further comprising:

encapsulating the IC die attached to the heat spreader the encapsulating further including placing a mold die against the sheet including against the heat spreader at a location near the edge of the heat spreader (**Fig. 3B**).

Regarding **claim 7**, Tsunoda discloses in col. **6**, lines **9-20**, a packaged integrated circuit (IC) comprising:

an IC die (**1**); a heat spreader (**5**), the IC die thermally coupled to the heat spreader at a first location of the heat spreader in a die up configuration, the heat spreader extends to at least a portion of an edge of the packaged IC (**Fig 1**).

Regarding **claim 8**, Tsunoda discloses in col. **6**, lines **23-31** wherein the heat spreader defines a wire bond window located between the first location and an outer portion of the heat spreader (**Fig 1**).

Regarding **claim 9**, Tsunoda discloses in col. **6**, lines **23-31** the packaged IC further comprising:

a wire bond extending from a die bond pad on the IC die into the wire bond window to a wire bond finger.

Regarding **claim 15**, Tsunoda discloses the claimed subject matter as stated above. Claim 15 is a combination of claim 1 and claim 5.

Regarding **claim 19**, Tsunoda discloses in **Fig 4B (b)** wherein the reducing the thickness of the sheet further includes coining a portion of the sheet at the location at the edge.

Regarding **claim 20**, Tsunoda discloses in **Fig 1** wherein the forming a heat spreader further includes forming a first singulation slot in the sheet and forming a second singulation slot in the sheet generally orthogonal with respect to the first singulation slot, wherein the location extends from the first singulation slot to the second singulation slot.

Regarding **claim 21**, Tsunoda discloses in **Fig 1** wherein the edge of the heat spreader includes four sides, wherein the location at the edge of the heat spreader is located along at least a majority of a side of the four sides.

Regarding **claim 22**, Tsunoda discloses in **Figs 1-4**:

the forming a heat spreader in the sheet further includes forming a plurality of heat spreaders in the sheet;

wherein the reducing the thickness of the sheet at a location at an edge of the heat spreader further includes reducing the thickness of the sheet at a plurality of locations with each location of the plurality at an edge of two adjacent heat spreaders of the plurality of heat spreaders;

wherein the attaching an IC die to the heat spreader further includes attaching each of a plurality of IC die to each of the plurality of heat spreaders at a first location of the each of the heat spreader;

encapsulating at least a portion of a first side of the sheet including encapsulating the plurality of IC dies in an encapsulate;

wherein the singulating the heat spreader with the attached IC die from a remaining portion of the sheet further includes singulating the plurality of heat spreaders with an attached IC die of the plurality of IC die, wherein the cutting the sheet at the location at the edge of the heat spreader further includes cutting the sheet of at the plurality of locations and cutting the encapsulate at locations above the plurality of locations.

Regarding **claim 23**, Tsunoda discloses in **Fig 4B (b)** wherein the location is at a corner of the heat spreader.

Regarding **claim 24**, Tsunoda discloses in **Fig 4B (b)** wherein the reducing the thickness of the sheet at the location at the edge of the heat spreader further includes reducing the thickness of the sheet at a plurality of locations at the edge wherein each location of the plurality is at a comer of the heat spreader.

Regarding **claim** ~~24~~ 25, Tsunoda discloses in **Fig 2B** wherein:

the sheet has a strip form, the strip form having a length and a width;

the forming a heat spreader in a sheet further includes forming a plurality of heat spreaders in the sheet along the length of the sheet in a one deep configuration along the width.

Claims 15-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Glenn et al. US 6,281,568 B1 (Glenn).

Glenn discloses in **Figs 1** and **11** a method for making a packaged integrated circuit (IC) comprising:

forming a heat spreader (**20**) in a sheet of thermally conductive material, wherein the forming includes reducing the thickness of the sheet at a location at an edge of the heat spreader (col. **12**, lines **39-53**);

attaching an IC die (**52**) to the heat spreader at a first location of the heat spreader;

singulating the heat spreader with the attached IC die from a remaining portion of the sheet, wherein the singulating further includes cutting the sheet at the location at the edge of the heat spreader (col. **12**, lines **39-53**).

Regarding **claims 16-18**, Glenn discloses in col. **12**, lines **39-53**: wherein the reducing the thickness of the sheet further includes etching a portion of the sheet at the location at the edge; wherein the etching a portion of the sheet further includes etching a first planar side of the sheet at the location and not a second planar side of the sheet at the location, wherein the first planar side is opposite the second planar side; wherein the die is attached to the heat spreader at a second planar side of the sheet.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Seth Barnes whose telephone number is (571) 272-6008. The examiner can normally be reached on Monday thru Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SWB

02/27/07

Zandra V. Smith
Supervisory Patent Examiner
1 March 2007